Appln. No. 10/696,101 Amdt. dated August 11, 2006 Reply to Office Action of March 20, 2006

## **Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

## **Listing of Claims:**

- 1. (Currently amended) A delay transistor comprising:
- a substrate;
- a plurality of conduction channels embedded in the substrate;
- a plurality of active regions embedded in the substrate, the active regions alternating with the conduction channels;
  - a source contact coupled with first alternating active regions;
  - a drain contact coupled with second alternating active regions; and
- a gate structure overlaying the conduction channels, the gate structure being configured to receive an input external signal, wherein the gate structure is a single gate structure, and wherein the gate structure provides an RC delay to the input external signal and filters power and voltage spikes in the input external signal, the RC delay being of a sufficiently long duration so as to decrease the switching speed of the transistor and allow the gate structure to filter power and voltage spikes, wherein the delay transistor further comprises a plurality of diodes coupled with the single gate structure, the diodes being reversed biased, wherein the diodes contribute additional capacitance to the RC delay.
- 2. (Original) The delay transistor of claim 1 wherein the gate structure has a serpentine shape.
- 3. (Original) The delay transistor of claim 1 wherein the gate structure comprises polysilicon.
  - 4. Canceled.
- 5. (Original) The trimming circuit of claim 1 wherein the delay transistor is an NMOS transistor.

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**PATENT** 

6. (Original) The trimming circuit of claim 1 wherein the delay transistor is a PMOS transistor.

7-14 Canceled.